AMENDMENTS TO THE CLAIMS

The claims as listed below will replace all prior listings and presentations of claims in the above-identified application.

1-7 (CANCELLED)

8. (ORIGINAL) An integrated circuit package, comprising:

a die;

a die attach layer over the die; and

an array of solder balls over the die attach layer;

wherein the die attach layer has a coefficient of thermal expansion of less than about 106 ppm/°C.

9. (PREVIOUSLY PRESENTED) The integrated circuit package of Claim 8, further comprising a flexible tape connecting the array of solder balls to the die, wherein one end of the tape is located over the die attach layer, and another end of the tape is located over the die.

10. (ORIGINAL) The integrated circuit package of Claim 8, wherein the die attach layer has a thickness of between about 5 and 7 mils.

11. (ORIGINAL) The integrated circuit package of Claim 8, wherein the die attach layer is an epoxy modified with elastomeric material.

12. (PREVIOUSLY PRESENTED) The integrated circuit package of Claim 8, wherein the array is a ball grid array.

13. (PREVIOUSLY PRESENTED) The integrated circuit package of Claim 8, wherein the array is a tape ball grid array.

14. (PREVIOUSLY PRESENTED) The integrated circuit package of Claim 8, wherein the array is a micro ball grid array.

15. (PREVIOUSLY PRESENTED) An integrated circuit package, comprising:

a die;

a die attach layer over the die; and

an array of solder balls over the die attach layer;

wherein the die attach layer has a coefficient of thermal expansion of less than about 106 ppm/°C and a modulus of elasticity of less than about 126 ksi and greater than about 10 ksi.

16. (PREVIOUSLY PRESENTED) The integrated circuit package of Claim 15, further comprising a flexible tape connecting the array of solder balls to the die, wherein one end of the tape is located over the die attach layer, and another end of the tape is located over the die.

17. (PREVIOUSLY PRESENTED) A first level integrated circuit package, comprising:

a first level package including a chip;

an array of solder balls for connecting the first level package to a second level package;

an adhesive layer between the chip and the array of solder balls, the adhesive layer having a coefficient of thermal expansion of less than about 200 ppm/°C; and

a flexible tape connecting the array to the chip

wherein one end of the tape is located over the adhesive layer, and another end of the tape is located over the chip.

18. (ORIGINAL) The package of Claim 17, wherein the tape connects the array to the chip using μBGA technology.

19. (ORIGINAL) The package of Claim 17, wherein the adhesive layer has a coefficient of thermal expansion of less than about 150 ppm/°C.

20. (ORIGINAL) The package of Claim 17, wherein the adhesive layer has a coefficient of thermal expansion of less than about 100 ppm/°C.

21. (PREVIOUSLY PRESENTED) A first level integrated circuit package, comprising:

a first level package including a chip;

an array of solder balls for connecting the first level package to a second level package;

an adhesive layer between the chip and the array of solder balls, the adhesive layer having a coefficient of thermal expansion of less than about 200 ppm/°C; and

a flexible tape connecting the array to the chip, wherein one end of the tape is located over the adhesive layer, and another end of the tape is located over the chip;

wherein the adhesive layer has a modulus of elasticity of greater than about 10 ksi and less than about 126 ksi.

22. (ORIGINAL) The package of Claim 21, wherein the adhesive layer has a modulus of elasticity of greater than about 50 ksi.

23. (ORIGINAL) The package of Claim 22, wherein the adhesive layer has a modulus of elasticity of greater than about 100 ksi.

24. (CANCELLED)

25. (CURRENTLY AMENDED) An integrated circuit package, comprising:

a flexible substrate;

a chip;

a plurality of conductive terminals on the substrate;

a plurality of conductive leads electrically connecting the conductive terminals to the chip; and

a compliant material between the chip and the substrate, the compliant material having a modulus of elasticity of less than about 126 ksi and more than about 10 ksi at room temperature and a coefficient of thermal expansion of less than about 200 ppm/°C;

wherein the conductive terminals are provided over the compliant material.

26. (ORIGINAL) The integrated circuit package of Claim 25, wherein the plurality of conductive terminals includes an array of solder balls.

27. (ORIGINAL) The integrated circuit package of Claim 25, wherein the plurality of conductive leads includes TAB leads.

28. (PREVIOUSLY PRESENTED) The integrated circuit package of Claim 25, wherein the flexible substrate is a polyimide.

29. (PREVIOUSLY PRESENTED) The integrated circuit package of Claim 25, wherein the compliant material has a modulus of elasticity of less than about 126 ksi and greater than about 50 ksi.

30. (PREVIOUSLY PRESENTED) The integrated circuit package of Claim 25, wherein the compliant material has a modulus of elasticity of less than about 126 ksi and greater than about 100 ksi.